a second switch. The second switch has a first position to couple the gate of the transistor via the resistor to the source, and a second position to an open circuit, removing the resistor between the gate and source as indicated at **640**. Both switches may be controlled to switch to their first positions to minimize EMS effects of a broad frequency spectrum of noise. In still further embodiments, the switches may be independently actuated. This allows the capacitor to be used when higher frequency noise is expected, while the resistor is effective for lower frequency noise or biases.

The Abstract is provided to comply with 37 C.F.R. §1.72(b) to allow the reader to quickly ascertain the nature and gist of the technical disclosure. The Abstract is submitted with the understanding that it will not be used to interpret or limit the scope or meaning of the claims.

The invention claimed is:

1. A circuit comprising:
- a transistor having a source, drain, gate and electrode structure;
- a source terminal coupled to the source;
- a drain terminal coupled to the drain;
- a gate terminal coupled to the gate;
- an electrode terminal coupled to the electrode structure; and
- a switch coupled to the source, the gate, and the electrode terminal to selectively couple the electrode structure to the source or the gate.

2. The circuit of claim **1** wherein the gate is an active gate layer for turning the transistor on and off, and wherein the electrode structure is insulated from the gate layer and is coupled to the switch.

3. The circuit of claim **2** wherein the transistor is a MOS trench power transistor.

4. The circuit of claim **3** wherein the electrode structure is configurable to provide additional capacitance between the gate and source.

5. The circuit of claim **4** wherein the gate layer extends into a trench in the drain.

6. The circuit of claim **2** wherein the electrode structure is formed within a chip area corresponding to the gate layer.

7. The circuit of claim **2** wherein the switch is adapted to couple the electrode structure to the source or to the gate layer in response to a switch control signal to provide additional capacitance between the gate and source.

8. The circuit of claim **2** wherein the switch is adapted to couple the electrode structure to the source or to open in response to a switch control signal.

9. The circuit of claim **1** wherein the transistor is supported by a substrate and further comprising additional circuitry supported by the substrate.

10. A circuit comprising:
- a transistor having a source, drain, gate and electrode structure;
- a source terminal coupled to the source;
- a drain terminal coupled to the drain;
- a gate terminal coupled to the gate;
- an electrode terminal coupled to the electrode structure;
- a first switch coupled to the source terminal, the gate terminal and the electrode terminal to selectively couple one of the gate and electrode structure to the source; and
- a second switch coupled to the source terminal and the gate terminal to selectively couple a resistor between the gate and the source.

11. The circuit of claim **8** wherein the gate is an active gate layer for turning the transistor on and off and is coupled to the second switch, and wherein the electrode structure is insulated from the first gate layer and is coupled to the first switch.

12. The circuit of claim **11** wherein the first switch is adapted to couple the electrode structure to the source or to the gate layer in response to a switch control signal.

13. The circuit of claim **12** wherein the second switch is adapted to couple the resistor to the source or to open.

14. The circuit of claim **12** wherein the first switch couples the electrode structure to the source and the second switch couples the resistor between the gate layer and the source to keep the transistor in an off state.

15. The circuit of claim **11** wherein the first switch is adapted to couple the second gate layer to the source or to open in response to a switch control signal.

16. A method comprising:
- coupling a geometric capacitance formed from multiple integrated layers proximate a trench MOS transistor gate to a source of the trench MOS transistor by use of a first switch to help keep the transistor in an off state; and
- opening the first switch to remove the coupling of the geometric capacitance to allow the transistor to transition to an on state.

17. The method of claim **16** wherein the first switch has a first position to couple the geometric capacitance to the source and a second position that couples the geometric capacitance to the gate of the transistor or to an open circuit.

18. The method of claim **16** and further comprising selectively coupling an gate of the transistor via a resistor to the source by use of a second switch.

19. The method of claim **18** wherein the second switch has a first position to couple the gate of the transistor via the resistor to the source, and a second position to an open circuit.

20. The method of claim **19** and further comprising controlling both switches to their first positions to minimize EMS effects of a broad frequency spectrum of noise.

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